REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 8, 15, 23-38 are all the claims presently pending in the application. Claims 8, 15, 23-24, 26-27, 31-32 and 35 have been amended to more particularly define the invention. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 8, 15, 23-38 stand rejected under 35 U.S.C. § 112, first paragraph and claims 8, 15, 23-38 stand rejected on prior art grounds.

With respect to the prior art rejections, claims 8, 15, 24-27, 29-32 and 34-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795). Claim 28 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) and in further view of Brewer (US Patent No. 6,322,600). Claims 23, 33 and 36-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) as applied to claim 8 above, and further in view of Wolf ("Silicon Processing for The VLSI Era").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor substrate having a trench region including at least one trench, the trench having a single layer of seamless HDP oxide having an unpolished upper surface, and a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of seamless HDP

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oxide. Importantly, the upper surface of the HDP oxide and the upper surface of the non-trench region are planarized without etch-back.

Conventional substrates having shallow trench isolation (STI) regions require harsh etching or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate. In other words, the height of the filler material is substantially processed from an initial trench fill height.

The claimed substrate, on the other hand, includes a substrate in which the upper surface of the HDP oxide and the upper surface of the non-trench region are planarized without etch-back. Specifically, the claimed device does not require an etch-back or chemical mechanical polishing (CMP) step to planarize the trench and non-trench regions. Therefore, the claimed substrate helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions.

II. THE 35 U. S. C. 112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claims 8, 15 and 23-35 contain subject matter which was not adequately described in the original specification. Applicant submits, however, that these claims are adequately supported by the specification.

Specifically, Applicant notes that the term "non-nitrided" has been deleted from the claims.

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Zheng and Liao References

The Examiner alleges that Zheng would have been combined with Liao to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Zheng discloses a method for forming planarized oxide shallow trench isolation. In

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the Zheng method, a high density plasma (HDP) oxide layer is deposited in the isolation trenches. A layer of spin-on-glass is coated over the HDP oxide layer. The spin-on-glass layer and portions of the HDP oxide layer remaining are polished away so that the substrate is planarized (Zheng at Abstract).

Liao discloses a method of correcting the scratches caused by CMP. In the Liao method, a microscratch formed in an isolation trench caused by chemical mechanical polishing is corrected by forming a sacrificial layer on the damaged trench fill so that the micro-scratch is thus filled with the sacrificial layer. Using a hard mask as an etch stop, the sacrificial layer is etched back. Since the etching rate of the sacrificial layer is the same as or lower than the isolation trench material, the formation of the micro-scratch is suppressed during the etching back process (Liao at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), whereas Liao teaches a method of correcting the damage (e.g., microscratches) caused by CMP (Liao at col. 1, lines 13-17). Indeed, Zheng does not even recognize the surface damage (e.g., scratches, chatter marks) caused by CMP and, unlike Liao, does not take any action to correct the damage. Therefore, Liao specifically teaches that the Zheng device is defective. Clearly, these references teach away from each other so that no person of ordinary skill in the art would have considered combining the references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng by choosing a removal method taught by that will result in a substantially scratch free surface as taught by Liao with reasonable expectation of producing a trench fill with a planar surface with reduced surface flaws" which is insufficient to support the combination.

Moreover, contrary to the Examiner's allegations, none of these references teach or suggest "*wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back*" as recited in claims 8, 15 and 23. As noted

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above, conventional substrates having shallow trench isolation (STI) regions require harsh etch-back or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate. In other words, the surface of the substrate is difficult to planarize. (Application at page 2, lines 9-18).

The claimed substrate, on the other hand, in which the upper surface of the HDP oxide and the upper surface of the non-trench region are planarized without etch-back or CMP. (Application at page 12, lines 16-20; page 6, lines7-15; Figure 7). Specifically, the claimed device does not require etch-back or chemical mechanical polishing (CMP) to planarize the trench and non-trench regions (Application at page 12, lines 16-18). Therefore, the claimed device helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions (Application at page 12, line 20-page 13, line 1).

Applicant further notes that the substrates in the cited references teach are fabricated very differently from the novel substrate. Therefore, it would be likely be impossible for these references to form co-planar trench and non-trench regions without using etch-back or CMP. Therefore, it is unlikely that these references would form co-planar trench and non-trench regions, where the trench and non-trench regions are easily planarized.

In particular, Zheng clearly does not teach or suggest the claimed substrate. Indeed, Zheng does not even recognize at least one of the problems (e.g., scratches and chatter marks formed by processing) which the claimed invention is intended to address.

Further, Zheng specifically teaches an etch-back process for the HDP-Oxide (Zheng at Figure 5; col. 3, lines 15-20). This is clearly different from the claimed substrate which is not planarized by etch-back.

Specifically, Zheng teaches the deposition of HDP oxide 18 in the trench region (Zheng at col. 2, lines 43-63; Figure 3). Then, a layer of spin-on-glass (SOG) 20 is coated over the HDP oxide 18 (Zheng at col. 2, line 64-col.3, line 14; Figure 4). The SOG 20 and HDP oxide 18 are then etched back to form the device illustrated in Figure 5 having "between about 2000 and 3000 Angstroms of HDP oxide ... on the wide silicon nitride areas" (Zheng at col. 3, lines 15-20).

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Further, Zheng states that if a planarized structure as illustrated in Figure 6 is desired, then chemical mechanical polishing must be performed. Specifically, Zheng states that "the remaining spin-on-glass material and HDP oxide overlying the silicon nitride areas may be polished away using chemical mechanical polishing (CMP) ... resulting in the planarized shallow trench isolation illustrated in FIG. 6" (Zheng at col. 3, lines 21-25).

In other words, Zheng teaches overfilling the trench, then etching-back the surface of the HDP oxide, and then performing CMP to planarize the structure. This is clearly is contrary to at least one of the objectives of the claimed invention (e.g., to provide a planarized surface without etch-back or CMP).

Likewise, Liao does not teach or suggest the novel features of the claimed invention. Indeed, Liao teaches merely forming an oxide layer in a trench and on a mask layer 24 to form an isolation layer 30. Then, Liao uses CMP to planarize the isolation layer, forms a sacrificial layer to fill in the microscratches formed by the CMP, then planarizes the surface by etching (Liao at col. 2, lines 53-60; Figure 2E).

In other words, Liao clearly does not teach or suggest a substrate in which the upper surface of the HDP oxide and the upper surface of the non-trench region are planarized without etch-back or CMP. Therefore, Liao does not make up for the deficiencies of Zheng.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Brewer Reference

The Examiner alleges that Brewer would have been combined with Zheng and Liao to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Brewer discloses a planarization composition for chemical mechanical planarization of dielectric layers for semiconductor manufacture, and methods for using the planarization

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composition in the manufacture of semiconductor devices (Brewer at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), and Liao teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), whereas Brewer is merely directed to a planarization composition for CMP (Brewer at col. 1, lines 13-17). Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng and Liao by adding dopant to the oxide trench fill as suggested by Brewer to produce a trench fill of a desired dielectric constant" which is insufficient to support the combination.

Moreover, Brewer does not teach or suggest "*wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back*" as recited in claims 8, 15 and 23. As noted above, unlike trenches with processed upper surfaces, the claimed substrate, includes a trench (e.g., STI) having an upper surface which may be planarized with a surface of a non-trench region without etch-back or CMP (Application at page 6, lines7-15; Figure 7).

Specifically, the claimed device does not require etch-back or chemical mechanical polishing (CMP) to planarize the trench and non-trench regions (Application at page 12, lines 16-18). Therefore, the claimed device helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions (Application at page 12, line 20-page 13, line 1).

Clearly, Brewer does not teach or suggest these novel features. Indeed, Brewer is merely directed to a composition for chemical mechanical polishing and is unrelated to the claimed substrate.

Specifically, Brewer may disclose a trench region in a substrate (Brewer at Figure 7b).

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However, the whole point of Brewer is to improve a CMP process for forming a trench region (Brewer at col. 11, line 40- col. 12, line 22). Applicant notes that it is very unlikely that any person of ordinary skill in the art would rely upon Brewer whose primary objective is to improve a CMP process, to form the claimed invention having an important objective of eliminating a processing (e.g., etching and CMP) of the HDP oxide in the trench. Therefore, Brewer does not make up for the deficiencies of the other references.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Wolf Reference

The Examiner alleges that Brewer would have been combined with Zheng, Liao and Philipossian to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Wolf discloses a boron-doped trench filler material (Wolf at page 48).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), and Liao teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), whereas Wolf is merely directed to a boron-doped trench fill. Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng and Liao by having dopants such as boron as taught by Wolf to be conventional practice, to produce an isolation trench that separates devices" which is insufficient to support the

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combination.

Moreover, Wolf does not teach or suggest "*wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back*" as recited in claims 8, 15 and 23. As noted above, unlike conventional trenches with processed upper surfaces, the claimed device does not require etch-back or chemical mechanical polishing (CMP) to planarize the trench and non-trench regions (Application at page 12, lines 16-18). Therefore, the claimed device helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions (Application at page 12, line 20-page 13, line 1).

Clearly, Wolf does not teach or suggest these novel features. Indeed, Wolf specifically teaches a reactive ion etch on the oxide trench fill (Wolf at page 48, Figure (f)).

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 8, 15 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: 2/28/03

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner David Blum, Group Art Unit # 2813 at fax number (703) 872-9319 this 28th day of February, 2003.

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

8. (Four Times Amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of [non-nitrided] seamless HDP oxide [filler material] having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said [non-nitrided] seamless HDP oxide, [filler material]

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

15. (Five Times Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of [non-nitrided] seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said [non-nitrided] seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants, and

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

23. (Five Times Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of [non-nitrided] seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said [non-nitrided] seamless HDP oxide,

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wherein said upper surface of said non-trench region comprises implanted dopants, and

wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.

24. (Amended) The semiconductor substrate according to claim 8, wherein said [filler material comprises] high density plasma oxide comprises non-conformal high density plasma oxide.

26. (Amended) The semiconductor substrate according to claim 8, wherein said [filler material comprises non-conformal] high density plasma oxide comprises a dopant.

27. (Amended) The semiconductor substrate according to claim 1 [24], wherein said high density plasma oxide comprises silicon dioxide.

31. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of [non-nitrided] seamless HDP oxide [filler material] and said upper surface of said non-trench region are planarized without chemical mechanical polishing.

32. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of [non-nitrided] seamless HDP oxide [filler material] is substantially scratch-free.

35. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of seamless HDP oxide [filler material] is free of chatter marks.

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